

<b>A/D CONVERTER (16-bit resolution)</b>	<b>MODEL</b>	<b>AD3V</b>
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**BEFORE USE ....**

Thank you for choosing us. Before use, please check contents of the package you received as outlined below. If you have any problems or questions with the product, please contact our sales office or representatives.

**■ PACKAGE INCLUDES:**

Signal conditioner  
(body + base socket + input resistor).....(1)  
Input resistor is provided only with current input type.

**■ MODEL NO.**

Confirm Model No. marking on the product to be exactly what you ordered.

**■ INSTRUCTION MANUAL**

This manual describes necessary points of caution when you use this product, including installation, connection and basic maintenance procedures.

**POINTS OF CAUTION**

**■ CONFORMITY WITH EU DIRECTIVES**

- This equipment is suitable for Pollution Degree 2 and Installation Category II (transient voltage 2500V). Reinforced insulation (signal input or output to power input: 300V) and basic insulation (signal input to output: 300V) are maintained. Prior to installation, check that the insulation class of this unit satisfies the system requirements.
- Altitude up to 2000 meters.
- The equipment must be mounted inside a panel.
- Insert a noise filter for the power source connected to the unit. TDK-Lambda Noise Filter Model RSNA-2006 or equivalent is recommended.
- The equipment must be installed such that appropriate clearance and creepage distances are maintained to conform to CE requirements. Failure to observe these requirements may invalidate the CE conformance.
- The actual installation environments such as panel configurations, connected devices, connected wires, may affect the protection level of this unit when it is integrated in a panel system. The user may have to review the CE requirements in regard to the whole system and employ additional protective measures\* to ensure the CE conformity.
- \* For example, installation of noise filters and clamp filters for the power source, input and output connected to the unit, etc.
- Install lightning surge protectors for those wires connected to remote locations.

**■ POWER INPUT RATING & OPERATIONAL RANGE**

- Locate the power input rating marked on the product and confirm its operational range as indicated below:  
100 – 240V AC rating: 85 – 264V, 47 – 66 Hz, approx. 10VA  
12 – 24V DC rating: 10.8 – 26.4V, approx. 4W  
110V DC rating: 85 – 150V, approx. 4W

**■ GENERAL PRECAUTIONS**

- Before you remove the unit from its base socket or mount it, turn off the power supply and input signal for safety.

**■ ENVIRONMENT**

- Indoor use.
- When heavy dust or metal particles are present in the air, install the unit inside proper housing with sufficient ventilation.
- Do not install the unit where it is subjected to continuous vibration. Do not subject the unit to physical impact.
- Environmental temperature must be within -5 to +55°C (23 to 131°F) with relative humidity within 30 to 90% RH in order to ensure adequate life span and operation.

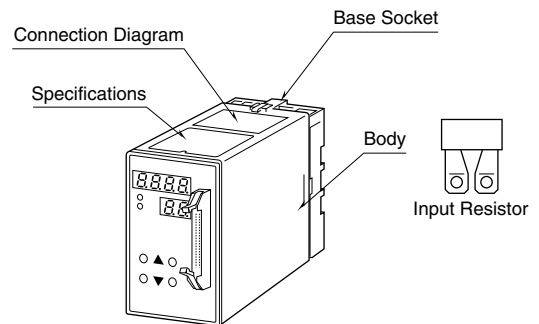
**■ WIRING**

- Do not install cables close to noise sources (relay drive cable, high frequency line, etc.).
- Do not bind the unit's cables together with cables where high noise levels are present. Do not install them in the same duct.

**■ AND ....**

- The unit is designed to function as soon as power is supplied, however, a warm up for 10 minutes is required for satisfying complete performance described in the data sheet.

**COMPONENT IDENTIFICATION**

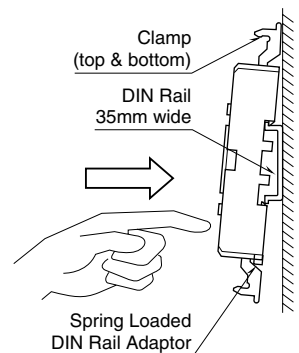


**INSTALLATION**

Detach the yellow clamps located at the top and bottom of the unit for separate the body from the base socket.

**■ DIN RAIL MOUNTING**

Set the base socket so that its DIN rail adaptor is at the bottom. Hang the upper hook at the rear side of base socket on the DIN rail and push in the lower. When removing the socket, push down the DIN rail adaptor utilizing a minus screwdriver and pull.



**■ WALL MOUNTING**

Refer to "EXTERNAL DIMENSIONS."

Shape and size of the base socket are slightly different with various socket types.

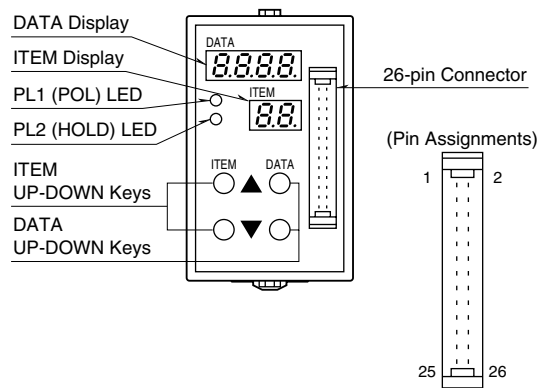
## FRONT PANEL CONFIGURATION & PROGRAMMING

### PROGRAMMING PROCEDURE

- 1) Press ITEM UP or DOWN key until ITEM display indicates "01".
- 2) Press DATA UP or DOWN key and choose "2" on DATA display.
  - 1 : Data indication only.
  - 2 : All parameters are modifiable.
- 3) Press ITEM UP or DOWN key until ITEM display shows the ITEM No. you need to change.
- 4) Press DATA UP or DOWN key and choose a DATA No. or value you need on DATA display.
- 5) Repeat above 3 and 4. (Entered data is stored when you move to a new ITEM.)
- 6) Press ITEM UP or DOWN key until ITEM display indicates "01".
- 7) Press DATA UP or DOWN key and choose "1" on the display.
- 8) Press ITEM UP or DOWN key until ITEM display indicates "P".
 

DATA display shows process input. You can now check data setting by choosing ITEM No.

Note : DO NOT press UP and DOWN keys simultaneously.



ITEM	MDF. CODE	DATA	CONTENTS	DEFAULT
P/L	N/A	-9999 – 9999 (-FFFF – FFFF)	Output display in engineering unit with ITEM 01 DATA 1 (as set in ITEM 06/07) Loop test output with ITEM 01 DATA 2 ('L' is indicated as ITEM No.) BCD or binary (with polarity), offset binary, two's complement, reflected binary	----
01		1, 2, 3	Modification code 1 : Data indication only. 2 : All parameters are modifiable. 3 : Only ITEM 24 is modifiable.	1
02	N/A	0 – 99	Status indication ("0" is normally indicated.) 0: Normal 1: Memory error 10: Out of input range -15 – +115%	0
03	N/A	-15.0 – 115.0	Input indicated in % (of the range set in ITEM 22/23)	----
04	2	-99.99 – 99.99	Zero adjustment (%) (fine adj. of the value set in ITEM 22)	0.00
05	2	-99.99 – 99.99	Span adjustment (%) (fine adj. of the value set in ITEM 23)	0.00
06	2	-9999 – 9999	BCD Display range scaling 0% *1	-1000
07	2	-9999 – 9999	Display range scaling 100% *1	1000
06	2	-7FFF – 7FFF	Binary Display range scaling 0% *1	-7FFF
07	2	-7FFF – 7FFF	Display range scaling 100% *1	7FFF
06	2	0000 – FFFF	Offset binary Display range scaling 0% *1	0000
07	2	0000 – FFFF	Display range scaling 100% *1	FFFF
06	2	8000 – 7FFF	Two's complement Display range scaling 0% *1	8000
07	2	8000 – 7FFF	Display range scaling 100% *1	7FFF
06	2	0000 – FFFF	Reflected binary Display range scaling 0% *1	0000
07	2	0000 – FFFF	Display range scaling 100% *1	FFFF
08	2	0 – 99	Power ON-delay time (seconds)	5
09	2	0, 1, 2, 3, 4	Display code 0 : BCD with polarity (decimal) 1 : Binary with polarity 2 : Offset binary 3 : Two's complement 4 : Reflected binary	0
10	2	0, 1, 2, 3, 4	Available number of bits 0: 16 bits 1: 14 bits 2: 12 bits 3: 10 bits 4: 8 bits	0
11	2	0, 1, 2	Parity check 0: Disable 1: Enable Parity per each digit 2: Enable Parity for all digits	0
12	2	0, 1	Odd or even parity (Checking the number of high in the output.) 0 : Odd (CMOS level, open collector (PNP) ), Even (open collector (NPN) ) 1 : Even (CMOS level, open collector (PNP) ), Odd (open collector (NPN) )	0
13	2	0, 1	POL, OVF output logic 0 : Data available at High (CMOS level) or ON (open collector) 1 : Data available at Low (CMOS level) or OFF (open collector)	0
14	2	0, 1	Data output logic *2 0 : Positive (CMOS level, open collector (PNP) ), Negative (open collector (NPN) ) 1 : Negative (CMOS level, open collector (PNP) ), Positive (open collector (NPN) )	0
15	2	0, 1	HOLD input logic 0 : HOLD at Low or shortcircuit 1 : HOLD at High or opencircuit	0

ITEM	MDF. CODE	DATA	CONTENTS	DEFAULT
16	2	0, 1	DAV output logic 0 : Data available at High (CMOS level) or ON (open collector) 1 : Data available at Low (CMOS level) or OFF (open collector)	0
17	2	1 – 50	DAV output time (msec.) selectable up to 50% of the Output Rate (ITEM 20)	1
18	2	0, 1, 2, 3, 4, 5	Moving average (10 msec./sampling) 0: No 1: 5 samples 2: 8 samples 3: 12 samples 4: 20 samples 5: 36 samples	1
19	2	0.0 – 60.0	Delay buffer (seconds, 0 – 90%) * When setting to less than or equal to 0.1, response time is 0.15 seconds.	0.5
20	2	1 – 20	Output rate 'n' ratio (n : 1 – 20 times)	1
21	2	0, 1 – 60	Power-saving mode 0 : Continuous display 1 – 60 : Time before display turned off (minutes)	10
22	2	-1.00 – 1.00	Input code S1 0% input voltage (V) *3 100% input voltage (V) *3	-1.00
23	2	-1.00 – 1.00		1.00
22	2	-10.0 – 10.0	Input code S2 0% input voltage (V) *3 100% input voltage (V) *3	-10.0
23	2	-10.0 – 10.0		10.0
22	2	-30.0 – 30.0	Input code S3 0% input voltage (V) *3 100% input voltage (V) *3	-30.0
23	2	-30.0 – 30.0		30.0
22	2	0.0 – 50.0	Input code Z1 0% input current (mA) *3 100% input current (mA) *3	4.0
23	2	0.0 – 50.0		20.0
24	3	0, 1	Reset all settings *4	0
25	N/A	----	ROM version	----

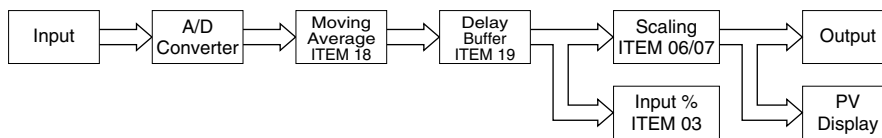
\*1. Of the range set in ITEM 04/05. ITEM 06 < ITEM 07.

\*2. ITEM 13, 15 or 16 is independent from ITEM 14.

\*3. ITEM 22 < ITEM 23.

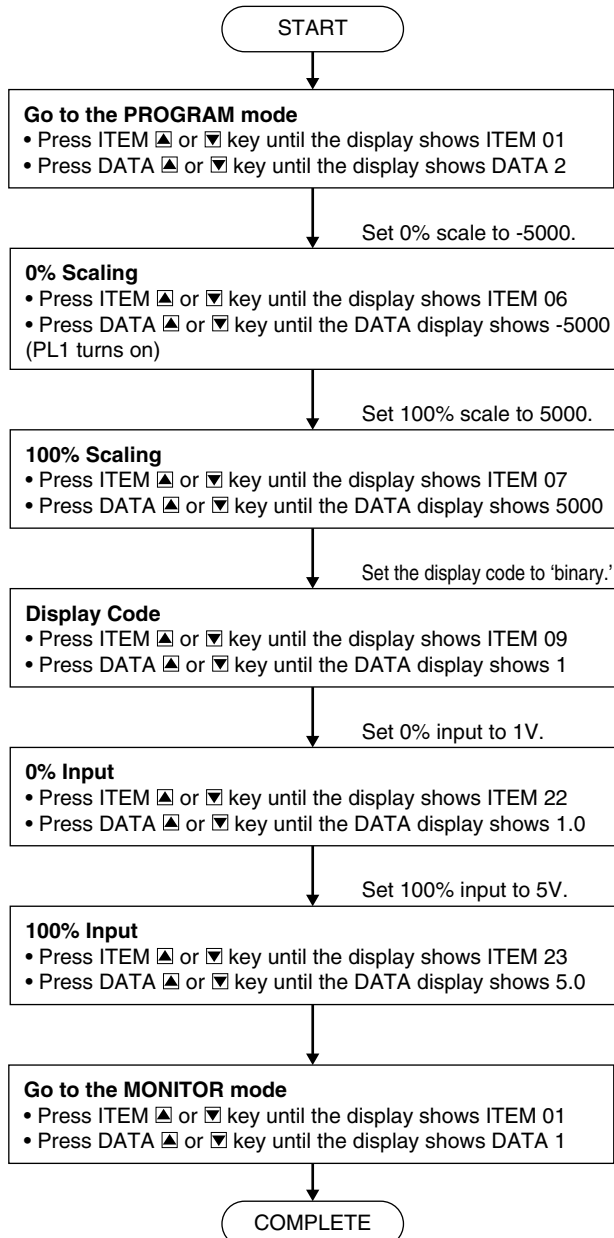
\*4. Press DATA UP key and choose DATA 1. Double-click DATA DOWN key. The display shows DATA 0 after the initialization is complete.

■ AD3V FUNCTION DIAGRAM



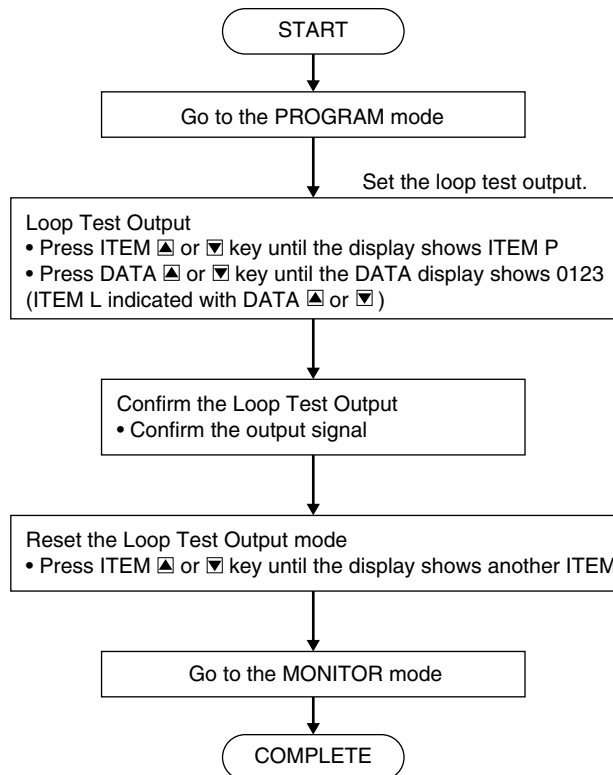
■ SELECTING SCALE, INPUT RANGE & OUTPUT TYPE

Setting orders may be changed.  
 [Example] Scale: -5000 to +5000  
 Input range: 1 to 5 V  
 Output type: Binary with polarity

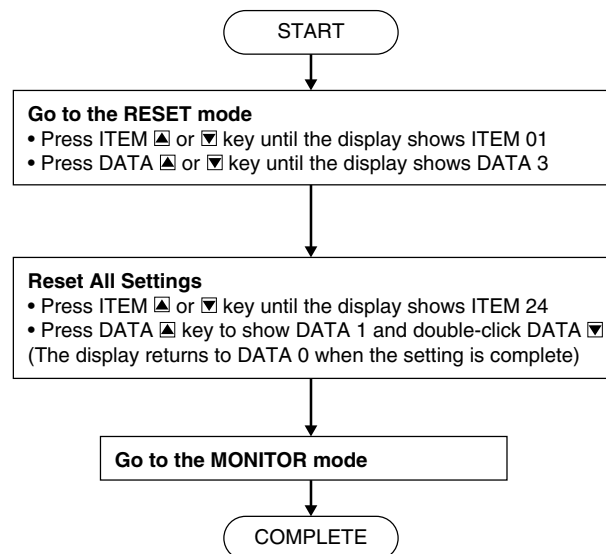


■ LOOP TEST OUTPUT

The loop test output is enabled when ITEM L (P) is selected in the PROGRAM mode.  
 [Example] Loop test output 0123



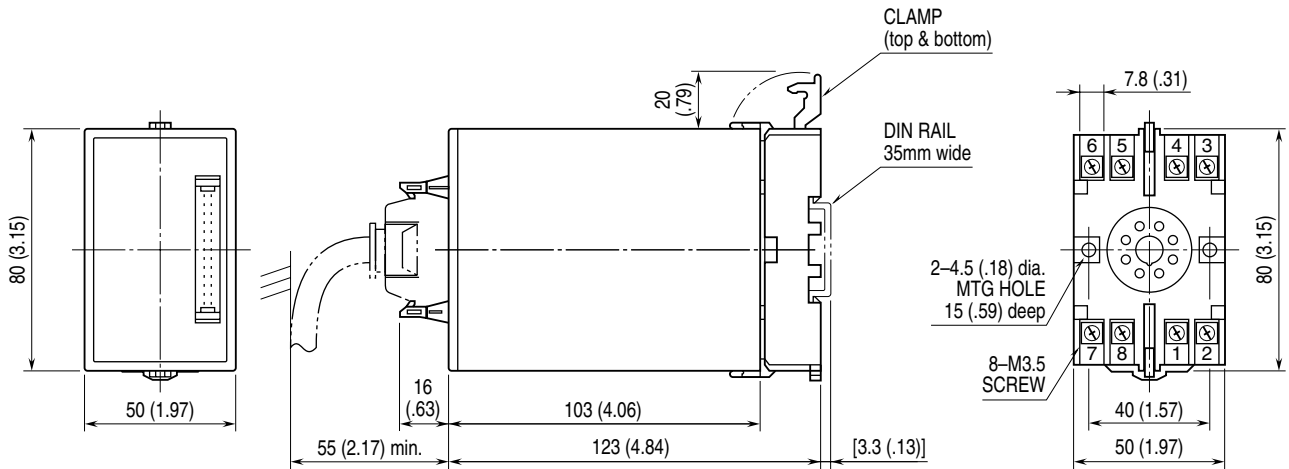
■ RESET ALL SETTINGS



## TERMINAL CONNECTIONS

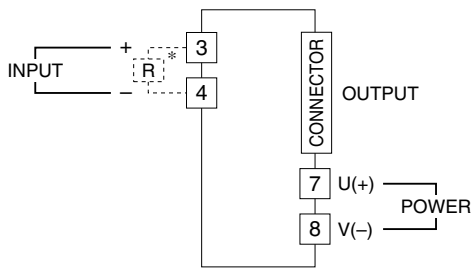
Connect the unit as in the diagram below or refer to the connection diagram on the top of the unit.  
When an input resistor is provided with the module, attach it together with input wiring to the input screw terminals.

### EXTERNAL DIMENSIONS unit: mm (inch)



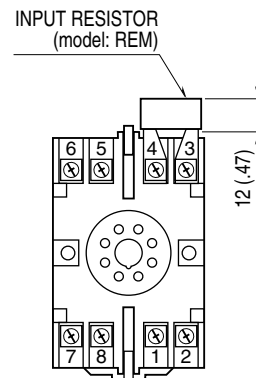
•When mounting, no extra space is needed between units.

### CONNECTION DIAGRAM



\*Input shunt resistor attached for current input.

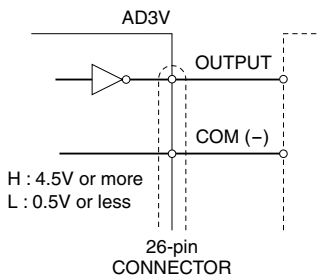
### TERMINAL ASSIGNMENT unit: mm (inch)



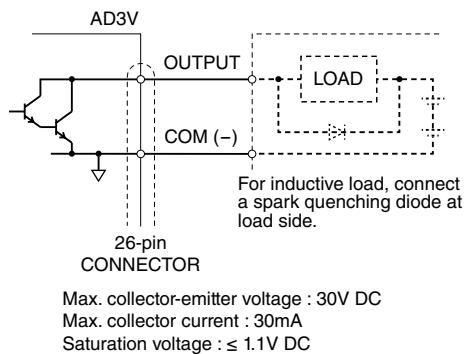
Input shunt resistor attached for current input.

## CONNECTION EXAMPLES

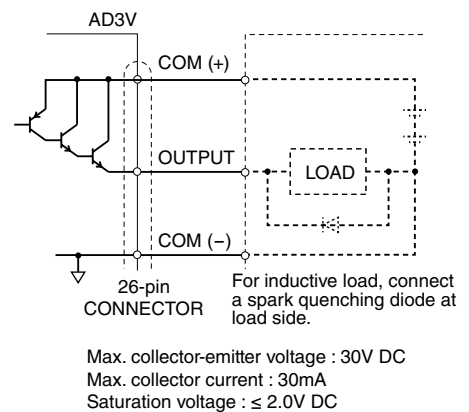
### • CMOS LEVEL (5V-CMOS)



### • OPEN COLLECTOR (NPN)



### • OPEN COLLECTOR (PNP)



## OUTPUT CONNECTOR (26-pin)

### BCD OUTPUT

PIN NO.	ASSIGNMENT	PIN NO.	ASSIGNMENT
1	$1 \times 10^0$	17	COM* <sup>1</sup>
2	$2 \times 10^0$	18	COM (-)
3	$4 \times 10^0$	19	OVF
4	$8 \times 10^0$	20	POL
5	$1 \times 10^1$	21	DAV
6	$2 \times 10^1$	22	HOLD* <sup>2</sup>
7	$4 \times 10^1$	23	P <sup>0</sup> * <sup>3</sup>
8	$8 \times 10^1$	24	P <sup>1</sup>
9	$1 \times 10^2$	25	P <sup>2</sup>
10	$2 \times 10^2$	26	P <sup>3</sup>
11	$4 \times 10^2$		
12	$8 \times 10^2$		
13	$1 \times 10^3$		
14	$2 \times 10^3$		
15	$4 \times 10^3$		
16	$8 \times 10^3$		

### BINARY, TWO'S COMPLEMENT OUTPUTS

PIN NO.	ASSIGNMENT	PIN NO.	ASSIGNMENT
1	B <sup>0</sup>	17	COM* <sup>1</sup>
2	B <sup>1</sup>	18	COM (-)
3	B <sup>2</sup>	19	OVF
4	B <sup>3</sup>	20	POL
5	B <sup>4</sup>	21	DAV
6	B <sup>5</sup>	22	HOLD* <sup>2</sup>
7	B <sup>6</sup>	23	P <sup>0</sup> * <sup>4</sup>
8	B <sup>7</sup>	24	P <sup>1</sup>
9	B <sup>8</sup>	25	P <sup>2</sup>
10	B <sup>9</sup>	26	P <sup>3</sup>
11	B <sup>10</sup>		
12	B <sup>11</sup>		
13	B <sup>12</sup>		
14	B <sup>13</sup>		
15	B <sup>14</sup>		
16	B <sup>15</sup>		

\*1. For open collector (NPN) and CMOS level, COM (-). For open collector (PNP), COM (+).

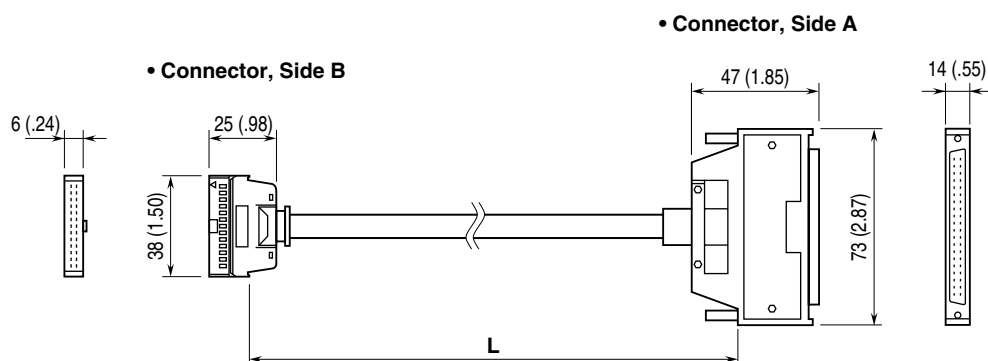
\*2. HOLD signal is for input, the others are for output.

\*3. P<sup>0</sup> corresponds to  $\times 10^0$ , P<sup>1</sup> to  $\times 10^1$ , P<sup>2</sup> to  $\times 10^2$ , P<sup>3</sup> to  $n \times 10^3$ . P<sup>0</sup> – P<sup>3</sup> are in sync when the parity for all digits are valid.

\*4. P<sup>0</sup> corresponds to B<sup>0</sup> – B<sup>3</sup>, P<sup>1</sup> to B<sup>4</sup> – B<sup>7</sup>, P<sup>2</sup> to B<sup>8</sup> – B<sup>11</sup>, P<sup>3</sup> to B<sup>12</sup> – B<sup>15</sup>. P<sup>0</sup> – P<sup>3</sup> are in sync when the parity for all digits are valid.

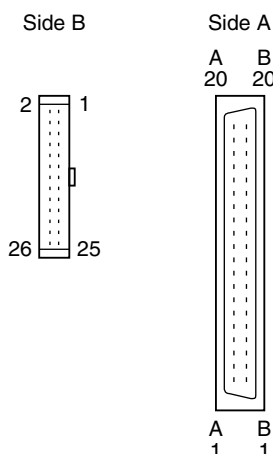
Note: With the number of bits set to 14 (or 12, 10, 8) with ITEM 10, Pin No. 1 – 14 (or 1 – 12, 1 – 10, 1 – 8) are valid.

## CABLE (MODEL: MCN26) PIN ASSIGNMENTS

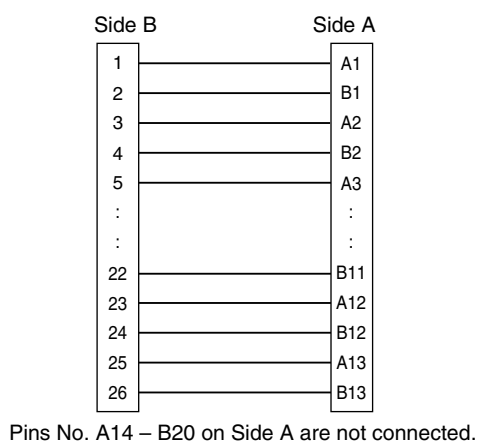


	MCN26-03	MCN26-05	MCN26-10	MCN26-30
L	30 cm (11.8 in.)	50 cm (19.7 in.)	1 m (3.3 ft.)	3 m (9.8 ft.)

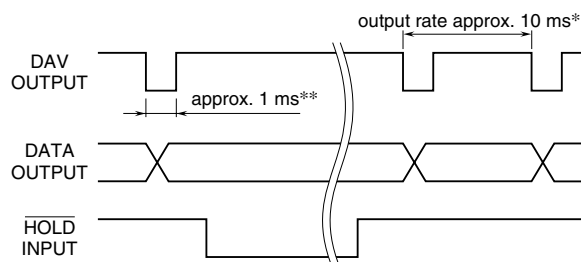
### CONNECTOR PIN ASSIGNMENT



### WIRING DIAGRAM



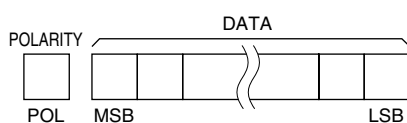
## TIMING CHART



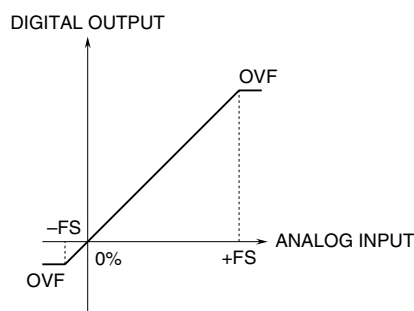
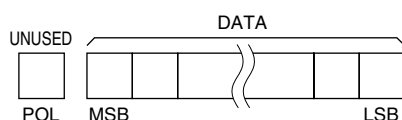
Data output is halt during  $\overline{\text{HOLD}}$  input.  
 DAV is output during DATA output.  
 \* Varies by individual module. Set to 'n' times with ITEM 20.  
 \*\*Selectable with ITEM 17.

## INPUT-OUTPUT RELATIONSHIP EXAMPLES

### ■ BCD, BINARY (WITH POLARITY)



### ■ OFFSET BINARY & TWO'S COMPLEMENT



#### • FS

-FS stands for -15 % of the input range, which is configured by ITEM 22, 0 % input voltage/current and ITEM 23, 100 % input voltage/current. +FS stands for +115 % of the input range.

#### • OVF

When one of the following conditions is true, the digital output overflows (OVF).

- 1) When the input signal is out of the range between -FS and +FS.
- 2) When the display value (= output signal) exceeds the display range.

The display range differs according to output code. For example, in case of BCD with polarity, it is -9999 to 9999. Please refer to the table in the FRONT PANEL CONFIGURATION & PROGRAMMING for detail.

## OUTPUT DATA & PARITY BIT RELATIONSHIP

Hi and Lo indicate the voltage level. Parity logic is unchanged. (ITEM 12 = I12; ITEM 14 = I14)

### ■ OPEN COLLECTOR (NPN)

#### • Positive Logic I14 : 1, Lo : False, Hi: True

DATA	8	4	2	1	PARITY	
					Even I12 : 0	Odd I12 : 1
0	Lo	Lo	Lo	Lo	Lo	Hi
1	Lo	Lo	Lo	Hi	Hi	Lo
2	Lo	Lo	Hi	Lo	Hi	Lo
3	Lo	Lo	Hi	Hi	Lo	Hi
4	Lo	Hi	Lo	Lo	Hi	Lo
5	Lo	Hi	Lo	Hi	Lo	Hi
6	Lo	Hi	Hi	Lo	Lo	Hi
7	Lo	Hi	Hi	Hi	Hi	Lo
8	Hi	Lo	Lo	Lo	Hi	Lo
9	Hi	Lo	Lo	Hi	Lo	Hi
10	Hi	Lo	Hi	Lo	Lo	Hi
11	Hi	Lo	Hi	Hi	Hi	Lo
12	Hi	Hi	Lo	Lo	Lo	Hi
13	Hi	Hi	Lo	Hi	Hi	Lo
14	Hi	Hi	Hi	Lo	Hi	Lo
15	Hi	Hi	Hi	Hi	Lo	Hi

#### • Negative Logic I14 : 0, Lo : True, Hi: False

DATA	8	4	2	1	PARITY	
					Even I12 : 0	Odd I12 : 1
0	Hi	Hi	Hi	Hi	Lo	Hi
1	Hi	Hi	Hi	Lo	Hi	Lo
2	Hi	Hi	Lo	Hi	Hi	Lo
3	Hi	Hi	Lo	Lo	Lo	Hi
4	Hi	Lo	Hi	Hi	Hi	Lo
5	Hi	Lo	Hi	Lo	Lo	Hi
6	Hi	Lo	Lo	Hi	Lo	Hi
7	Hi	Lo	Lo	Lo	Hi	Lo
8	Lo	Hi	Hi	Hi	Hi	Lo
9	Lo	Hi	Hi	Lo	Lo	Hi
10	Lo	Hi	Lo	Hi	Lo	Hi
11	Lo	Hi	Lo	Lo	Hi	Lo
12	Lo	Lo	Hi	Hi	Lo	Hi
13	Lo	Lo	Hi	Lo	Hi	Lo
14	Lo	Lo	Lo	Hi	Hi	Lo
15	Lo	Lo	Lo	Lo	Lo	Hi

### ■ CMOS LEVEL, OPEN COLLECTOR (PNP)

#### • Positive Logic I14 : 0, Lo : False, Hi: True

DATA	8	4	2	1	PARITY	
					Even I12 : 0	Odd I12 : 1
0	Lo	Lo	Lo	Lo	Hi	Lo
1	Lo	Lo	Lo	Hi	Lo	Hi
2	Lo	Lo	Hi	Lo	Lo	Hi
3	Lo	Lo	Hi	Hi	Hi	Lo
4	Lo	Hi	Lo	Lo	Lo	Hi
5	Lo	Hi	Lo	Hi	Hi	Lo
6	Lo	Hi	Hi	Lo	Hi	Lo
7	Lo	Hi	Hi	Hi	Lo	Hi
8	Hi	Lo	Lo	Lo	Lo	Hi
9	Hi	Lo	Lo	Hi	Hi	Lo
10	Hi	Lo	Hi	Lo	Hi	Lo
11	Hi	Lo	Hi	Hi	Lo	Hi
12	Hi	Hi	Lo	Lo	Hi	Lo
13	Hi	Hi	Lo	Hi	Lo	Hi
14	Hi	Hi	Hi	Lo	Lo	Hi
15	Hi	Hi	Hi	Hi	Hi	Lo

#### • Negative Logic I14 : 1, Lo : True, Hi: False

DATA	8	4	2	1	PARITY	
					Even I12 : 0	Odd I12 : 1
0	Hi	Hi	Hi	Hi	Hi	Lo
1	Hi	Hi	Hi	Lo	Lo	Hi
2	Hi	Hi	Lo	Hi	Lo	Hi
3	Hi	Hi	Lo	Lo	Hi	Lo
4	Hi	Lo	Hi	Hi	Lo	Hi
5	Hi	Lo	Hi	Lo	Hi	Lo
6	Hi	Lo	Lo	Hi	Hi	Lo
7	Hi	Lo	Lo	Lo	Lo	Hi
8	Lo	Hi	Hi	Hi	Lo	Hi
9	Lo	Hi	Hi	Lo	Hi	Lo
10	Lo	Hi	Lo	Hi	Hi	Lo
11	Lo	Hi	Lo	Lo	Lo	Hi
12	Lo	Lo	Hi	Hi	Hi	Lo
13	Lo	Lo	Hi	Lo	Lo	Hi
14	Lo	Lo	Lo	Hi	Lo	Hi
15	Lo	Lo	Lo	Lo	Hi	Lo

## CHECKING

- 1) Terminal wiring: Check that all cables are correctly connected according to the connection diagram.
- 2) Power input voltage: Check voltage across the terminal 7 – 8 with a multimeter.
- 3) Input: Check that the input signal is within 0 – 100% of the full-scale.
- 4) Output
  - Open collector: Check that the output load is 30V DC/30mA at the maximum. Saturation voltage for NPN transistor is 1.1V DC. Check the input threshold voltage (at L level) of the connected device to be greater than that.  
Saturation voltage for PNP transistor is 2.0V DC. Check the input threshold voltage (at H level) of the connected device to be 2V lower than COM (+) voltage.
  - CMOS level: Check the output voltage (H ≥ 4.5V DC, L ≤ 0.5V DC).

## LIGHTNING SURGE PROTECTION

We offer a series of lightning surge protector for protection against induced lightning surges. Please contact us to choose appropriate models.