

# ORDERING INFORMATION Model : A D 3 V

## PLEASE FILL IN THIS SECTION



Model
Company
Name
P/O No.

## FACTORY USE ONLY



Job No.	Approved by (Sales office)
Ser No. —	
Sales	Issued by (Sales office)

Specify the items you want to change.

Default setting will be used if not specified.

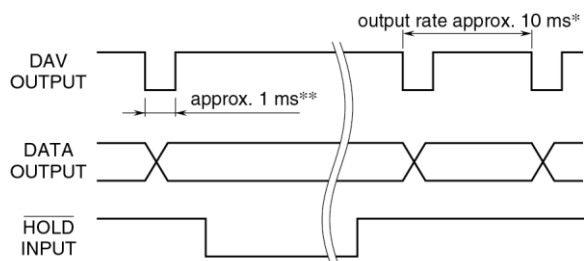
DEFAULT shows values in case of nothing specified.

### PROGRAMMABLE ITEMS

ITEM	CONTENTS	AVAILABLE VALUE	DEFAULT VALUE	SET VALUE Fill in this column
06	Display range scaling 0% (as set in ITEM 22/23)			
	BCD	-9999 to 9999	-1000	
	Binary	-7FFF to 7FFF	(-7FFF)	
	Offset binary / Reflected binary	0000 to FFFF	(0000)	
07	Two's complement	8000 to FFFF	(8000)	
	Display range scaling 100% (as set in ITEM 22/23)			
	BCD	-9999 to 9999	1000	
	Binary	-7FFF to 7FFF	(7FFF)	
08	Offset binary / Reflected binary	0000 to FFFF	(FFFF)	
	Two's complement	8000 to FFFF	(FFFF)	
09	Power ON-delay time	0 to 99 (sec.)	5 (sec.)	
10	Display code	0, 1, 2, 3, 4	0 : BCD with polarity (decimal)	
	0 : BCD with polarity (decimal)			
	1 : Binary with polarity			
	2 : Offset binary			
	3 : Two's complement			
11	4 : Reflected binary			
	Available number of bits	0, 1, 2, 3, 4	0 : 16 bits	
	0 : 16 bits			
	1 : 14 bits			
	2 : 12 bits			
12	3 : 10 bits			
	4 : 8 bits			
	Parity check	0, 1, 2	0 : Disable	
13	0 : Disable			
	1 : Enable Parity per each digit			
	2 : Enable Parity for all digits			
14	Odd or even parity (Checking the number of High in the output)	0, 1	0 : Odd (CMOS, open collector (PNP) ), Even (open collector (NPN) )	
	0 : Odd (CMOS, open collector (PNP) ), Even (open collector (NPN) )			
15	1 : Even (CMOS, open collector (PNP) ), Odd (open collector (NPN) )			
	POL, OVF output logic	0, 1	0 : Data available at High (CMOS) or ON (open collector)	
16	0 : Data available at High (CMOS) or ON (open collector)			
	1 : Data available at Low (CMOS) or OFF (open collector)			
17	Data output logic	0, 1	0 : Positive (CMOS, open collector (PNP) ), Negative (open collector (NPN) )	
	0 : Positive (CMOS, open collector (PNP) ), Negative (open collector (NPN) )			
	1 : Negative (CMOS, open collector (PNP) ), Positive (open collector (NPN) )			

ITEM	CONTENTS	AVAILABLE VALUE	DEFAULT VALUE	SET VALUE Fill in this column
15	HOLD input logic 0 : HOLD at Low or shortcircuit 1 : HOLD at High or opencircuit	0, 1	0 : HOLD at Low or shortcircuit	
16	DAV output logic 0 : Data available at High (CMOS) or ON (open collector) 1 : Data available at Low (CMOS) or OFF (open collector)	0, 1	0 : Data available at High (CMOS) or ON (open collector)	
17	DAV output time selectable up to 50% of the Output Rate (ITEM 20)	1 to 50 (msec.)	1 (msec.)	
18	Moving average (10 msec./sampling) 0 : No 1 : 5 samples 2 : 8 samples 3 : 12 samples 4 : 20 samples 5 : 36 samples	0, 1, 2, 3, 4, 5	1 : 5 samples	
19	Delay buffer (seconds, 0 – 90%) * When setting to less than or equal to 0.1, response time is 0.15 seconds.	0.0 to 60.0 (sec.)	0.5 (sec.)	
20	Output rate 'n' ratio (n : 1 – 20 times)	1 to 20	1	
21	Power-saving mode 0 : Continuous display 1 – 60 : Time before display turned off	0, 1 to 60 (min.)	10 (min.)	
22	0% input voltage/current (ITEM 22 < ITEM 23)	S1 : -1.00 to 1.00 S2 : -10.0 to 10.0 S3 : -30.0 to 30.0 Z1 : 0.0 to 50.0	S1 : -1.00V S2 : -10.0V S3 : -30.0V Z1 : 4.0mA	
23	100% input voltage/current (ITEM 22 < ITEM 23)	S1 : -1.00 to 1.00 S2 : -10.0 to 10.0 S3 : -30.0 to 30.0 Z1 : 0.0 to 50.0	S1 : 1.00V S2 : 10.0V S3 : 30.0V Z1 : 20.0mA	

## ■ TIMING CHART



Data output is halt during  $\overline{\text{HOLD}}$  input.  
DAV is output during DATA output.

\* Varies by individual module. Set to 'n' times with ITEM 20.

\*\*Selectable with ITEM 17.